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(56) Documents Cited

GB 2001197 A US 5495122 A US 4651406 A

(58) Field of Search

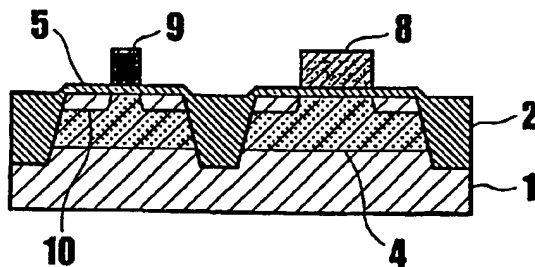
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(54) Abstract Title

Gate electrodes for integrated mosfets

(57) A plurality of MOSFETs of one conductivity type having gate electrodes 8,9 formed of a semiconductor material are formed in a semiconductor substrate 1. The gate electrodes of these MOSFETs are implanted with an impurity at different concentrations in accordance with the threshold voltages to be set for the MOSFETs. Initially, an isolation region 2 and wells 4 are formed on the surface of the semiconductor substrate. Then a gate oxide film 5 is formed on the surfaces of the isolation region and the well. A polysilicon film for forming gate electrodes is then grown on the surfaces of the gate oxide film and the isolation region. A resist is then deposited to allow ion implantation in one gate region of the polysilicon film but prevent implantation in the other gate region. After removing the resist and patterning the polysilicon film to form first and second gate electrodes 8,9 a second impurity is implanted in the first and second gate electrodes and prospective source/drain regions 10.

FIG. 3F



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